ARGUMENTS/REMARKS

STATUS OF CLAIMS

Claims 1 – 19 are pending.

Claims 1 – 2 are withdrawn from consideration.

Claims 3 – 19 stand rejected.

Rejection of claims 3-19

Claims 3 -19 stand rejected under 35 U.S.C. 103 as being unpatentable over U.S. Patent No. 6,294,801 (Inokuchi) in view of U.S. Patent No. 6,593,603 (Kim). The rejection is respectfully traversed, for at least the reason that the combination proposed by the Examiner would not result in an integrated circuit having all of the limitations of the rejected claims.

As to claim 3, the Examiner states that Inokuchi discloses a first block comprising an enhancement mode PHEMT transistor on a substrate, and a second block comprising a depletion mode PHEMT transistor on the substrate. The Examiner cites col. 11, lines 6-29, and Fig. 6 of Inokuchi. The Examiner concedes that Inokuchi fails to teach a power PHEMT transistor.

The Examiner states that Kim discloses a high electron mobility transistor with a third block comprising a power PHEMT transistor on the substrate, the third block operatively connected to at least one of the first block and the second block. The Examiner states that it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Inokuchi and Kim to form a transistor since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. The Examiner states that doing so would

facilitate the manufacture of the semiconductor device and enhance the performance of the semiconductor transistor.

The rejection of claim 3 is respectfully traversed for at least the reasons that: (1) the combination proposed by the Examiner would not result in the claimed integrated circuit, and (2) no valid grounds have been articulated that would render the proposed combination obvious to one of ordinary skill in the art.

Claim 3 recites:

3. An integrated circuit, comprising:
   a. a first block comprising an enhancement mode pHEMT transistor on a substrate;
   b. a second block comprising a depletion mode pHEMT transistor on the substrate, the second block operatively connected to the first block; and
   c. a third block comprising a power pHEMT transistor on the substrate, the third block operatively connected to at least one of the first block and the second block.

Claim 3 requires an enhancement mode PHEMT, a depletion mode PHEMT, and a power PHEMT, on the *same* substrate. As Inokuchi and Kim disclose different substrates, it is not possible to combine these references to obtain the integrated circuit of claim 3.

For example, the substrate of Kim has an AlGaAs/GaAs superlattice layer 14, i.e., a layer composed of alternating layers of AlGaAs and GaAs, formed on a GaAs buffer layer 12 (col. 4, lines 45-47). In contrast, the substrate of Inokuchi lacks a superlattice layer.

By way of further example, the substrate of Inokuchi has first and second doped silicon layers 20 and 28 separated from InGaAs electron transit layer 24 by spacers 22,

26, with the doping concentration of the first doped silicon layer 20 being twice that of the second doped silicon layer 28 (col. 4, lines 45-59). In contrast, the substrate of Kim, rather than include doped silicon layers, has a first electron supply layer 108 composed of n^+AlGaAs and second electron supply layer 116, composed of n^+AlGaAs separated by spacers from channel layer 112 of InGaAs (col. 4, lines 49-58). Thus, the electron supply layers in the respective substrates are of entirely different materials.

By way of still further example, the respective cap layers differ. The cap layer of Kim is doped GaAs (col. 4, lines 60-62). The cap layer of 32 of Inokuchi is undoped GaAs (col. 4, lines 66-67).

In short, the proposed combination is not possible, as Inokuchi and Kim teach two different substrates.

Furthermore, the proposed rationale for obviousness is not appropriate. The Examiner proposes to form a transistor. However, Inokuchi already teaches a transistor; accordingly, there is no need to modify Inokuchi to form a transistor. Furthermore, there is no duplication of components between Inokuchi and Kim, as the two references teach differing and non-duplicative substrates. Still further, there is no indication that the proposed modification would enhance manufacture of the semiconductor device. Since it is not possible to combine the differing substrates of Inokuchi and Kim, there is no obvious enhancement of the manufacture of devices.

In short, the Examiner has failed to provide a proper prima facie case of obviousness as to claim 3.

For at least the foregoing reasons, claim 3 is allowable over the prior art of record.

Claim 4 depends from claim 3 and recites, inter alia, a clock input, an analog input, and a digital input, wherein the first and second block connect to form an analog to digital converter. The Examiner points to Figure 6 of Inokuchi as teaching these limitations. However, Figure 6 is merely a partial sectional view of a PHEMT, and does not show any of a clock input, an analog input or a digital input.

For this reason, as well as the reasons set forth above in connection with claim 3, claim 4 is allowable over the prior art of record.

Claim 5 depends from claim 3, and adds the further limitation that the integrated circuit is a microwave and millimeter wave integrated circuit (MMIC). The Office Action refers to Figure 6 of Inokuchi. As noted above, Figure 6 of Inokuchi is merely a partial cross section of a PHEMT, and does not disclose an MMIC. For at least this reason, as well as the reasons set forth above in connection with claim 3, claim 5 is allowable.

Claim 6 depends from claim 3, and adds the further limitation that the integrated circuit is capable of operating at a frequency within the range of from very low frequency up to and including X-band frequencies. In order for this limitation to be taught in the prior art, a reference must teach a circuit capable of operating at this entire frequency range; a circuit capable of operating at only a portion of this range does not teach the limitations of claim 6. The Office Action again refers to Figure 6 of Inokuchi for this limitation. However, as noted, Figure 6 of Inokuchi merely discloses a partial cross section of a PHEMT, and does not teach integrated circuits. For at least this reason, as well as the reasons set forth above in connection with claim 3, claim 6 is allowable.

Claim 7 is an independent claim reciting an analog to digital converter, having an enhancement mode pHEMT device, a depletion mode pHEMT device, and a power pHEMT device on a single substrate. For the reasons discussed above in connection with claim 3, the Examiner has not provided a proper prima facie case of obviousness as to these three types of devices formed on a single substrate. For at least this reason, claim 7 is allowable.

Claims 8 and 9 depend from claim 7, and are allowable for the reasons that claim 7 is allowable.

Claim 10 is an independent claim that includes all of the limitations of claim 3, and is allowable for the reasons that claim 3 is allowable.

Claims 11 – 15 and 17 - 19 depend directly or indirectly from claim 3, and are allowable over the prior art of record at least for the reasons set forth above in connection with claim 3.

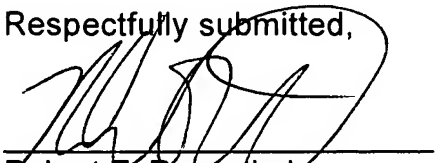
Claim 16 depends indirectly from claim 3, and further recites that the recess of the power pHEMT transistor is a double recess, that the recess of the depletion mode pHEMT transistor is a single recess, and that each of the recesses is defined through at least one common layer of the substrate. There is no teaching or suggestion in either Inokuchi or Kim of a power pHEMT transistor having a double recess and a depletion mode pHEMT transistor having a single recess, each of those recesses defined through at least one common layer of a substrate. For at least these reasons, as well as the reasons set forth above in connection with claim 3, claim 16 is allowable.

CONCLUSION

Wherefore, Applicant believes he has addressed all outstanding matters, and respectfully requests that claims 3 – 19 be allowed.

Should there be any questions or outstanding matters, the Examiner is cordially invited and requested to contact Applicant's undersigned attorney at his number listed below.

Respectfully submitted,



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